EE/CprE/Se 492 Weekly Report 4
2/28/25 - 3/13/25
sdmay25-28
Digital ASIC fabrication
Client & Advisor: Dr. Duwe

Team Members
Calvin Smith – Accelerator Design lead
Camden Fergen – DevOps and Project Lead
John – Testing Lead
Nicholas – Harden and Verification lead
Levi – Communication Interfaces Lead

Weekly Summary

This week, progress was made across multiple areas, including adapting processing elements for improved memory interfacing and constructing a direct memory access system for more efficient data loading. Work continued on the CICD pipeline, with advancements in setting up a Docker-based environment, though some toolchain issues remain. Efforts were also directed toward implementing new instructions, such as dot product computation and FFT. Challenges arose in setting up a proper cross-compiler for a bare-metal system, requiring research and troubleshooting to resolve unexpected library path issues. Additionally, memory controller integration with the SPI main unit was completed, and successful tests were conducted for writing instructions into memory through the Wishbone interface

Pask Week Accomplishments

- Calvin:
    - Adapted previous processing elements for use with the CyDMA
    - Began construction of the CyDMA itself for directly interfacing with memory in the CyGRA for much timelier data loading
    - Created a priority memory bus splitter interface to allow for the pico and CyDMA to share the single memory interface offered by the cache
- Camden:
    - Continued work on the CICD pipeline mainly focusing on the pico processor as that is the most important to ensure everything is working
    - Was able to get the docker image built so that it easy to bull when needing to run the pipeline with the gitlab runner

    - Still running into a few issues with that so still not fully resolved, but further progress on it is being made. May need to revise and ensure correct toolchain is installed
- John:
    - I started writing an instruction that would compute the dot product
    - Also started working on FFT instruction
- Levi:
    - Worked on getting a riscv32ui cross compiler setup on the vm, thought this was a solved issue last week however it turns out the compiler that was thought to have worked was targeting linux systems and not a baremetal system which needs an unknown-elf-gcc compiler. This meant I had to research and follow guides to build a compiler and found extensive issues where the compiler is not able to locate or expects libraries to be found in directories where they're not.
- Nicholas:
    - Finished interfacing memory controller with SPI main unit.
    - Integrated SPI main unit into caravel project.
    - Successfully tested writing instructions into memory through the wishbone slave.

Name	Individual Contribution	Hours this Week	Hours Cumulative
Calvin	• CyDMA progress • Memory interface splitter • PE adaptation	10	110.044
Camden	• Semi working CICD pipeline • Docker image with riscv toolchain installed	20	100
John	• Dot product instruction • FFT instruction	10	110
Levi	• Worked on getting cross compiler running	8	90

	(for real) this time		
Nicholas	• SPI main integration • Testing Caravel Project	10	116

Plans for Upcoming Week

- Calvin:
  - Enjoy spring break
  - Try to get motivation back after the loss of efabless
  - Hopefully get the CyDMA to a mildly functioning state
- Camden:
  - Enjoy even more spring break and cry about 488
  - Hopefully get CICD pipeline working for pico processor
- John:
  - Keep working with CyGRA and helping with the implementation of the benchmarks
- Levi:
  - Finally get to FPGA testing! Make my body a machine that turns my free hours over spring break into script running and log analysis.
- Nicholas:
  - Add support for external instruction memory.
  - Fully test Caravel project in software.
  - Prep for FPGA testing.

Summary of weekly advisor meeting

Between the two status reports, we have had two meetings with our advisor. Our first meeting we discussed testing and agreed on using Chip Forge's testing platform for Caravel projects. Dr. Duwe also gave us an overview of testing with Chip Forge's tools so we can test on an FPGA when our Caravel projects are ready. Our second meeting we discussed first discussed eFabless going bankrupt and how it would affect our project. Dr. Duwe said we should continue as if eFabless still exists. benchmarks, specifically adapting our benchmarks to work with our project, Dr. Duwe gave us some pointers that will help us do this. We also discussed preparing for a Caravel simulation on an FPGA, which we are close to achieving and should allow us to run our benchmarks.